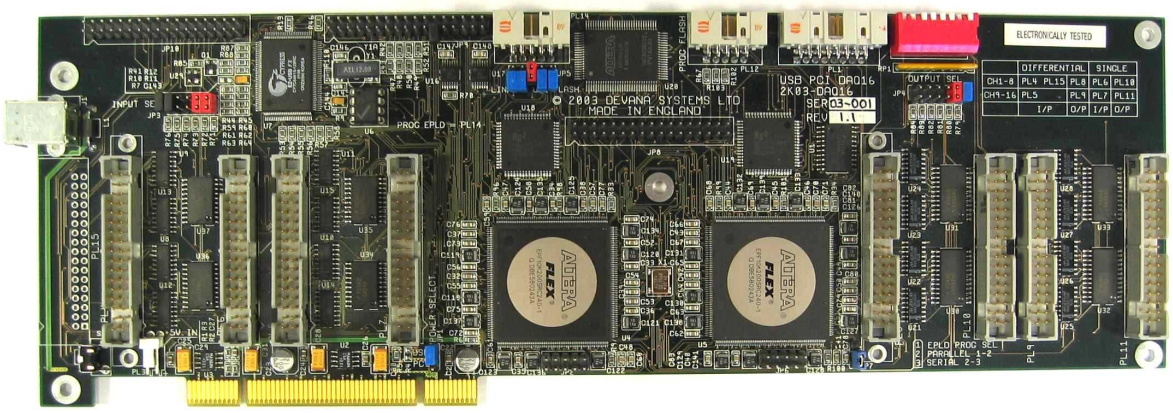
Devana Systems

Hardware User Manual

PCI-DAQ16
16 channel Digital Sonobuoy Data Acquisition Board



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Document Revision

Version from	Version to	Details
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1.00	1.01	Specification of the faster serial rate para 7.1
1.01	1.02	Defined 2nd byte of START_ACQ command para 8.2, updated command sequence explanation
1.02	1.03	Correct FIFO size to 512kB per 8 channels, serial test mode signaled by Yellow LED ON
1.03	1.04	FPGA_CONFIG command – default page is 0 and alternative configuration is stored in page 1. Section 8.2 updated.
1.04	2.00	ADAR buoy specific
2.00	2.01	Normal user not required to program Flash PROM or FPGA
2.01	3.00	Upgraded firmware and commands to check FPGA configuration image and select input and output signal type via USB command
3.00	4.00	Output mode added, checksum calculated before XORing data
4.00	4.10	Remove buoy specific formatting information – make generic user manual. Tidy up version error.
4.10	5.10	Add DVLA_RDT Mode – Not issued
5.10	6.00	Add user configurable XOR bit mask for specific data fields
6.00	7.00	Tidy up document references – update USB driver info

HW User Manual: PCI DAQ16 Board

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1 Functional Overview

The 16 Channel PCI Sonobuoy Data Acquisition (DAQ) Board, with USB v1.1 interface, accepts data from 16 digital sonobuoys, and performs bit and frame synchronization, data and compass de-multiplexing in real-time. The input data stream can be digital or analogue and single-ended or differential. The data streams may be Non-Return to Zero (NRZ) with or without clock, Miller/ Delayed Modulation Mark (DMM) or Manchester encoded. Each channel is bit-synchronized independently; this ensures that data from sonobuoys operating at different data rates (but still within specification) is reliably acquired. Bit synchronized, single-ended and/or RS422 compatible differential, output NRZ data and clock signals are generated for each channel. These signals may be used to feed external data recorders or monitors.

Buoy specific signal formatting and decoding information is included in the buoy format specification document.

The DAQ board is controlled via commands sent over the USB interface from the PC.

Figure 1 illustrates the DAQ board interfaces.

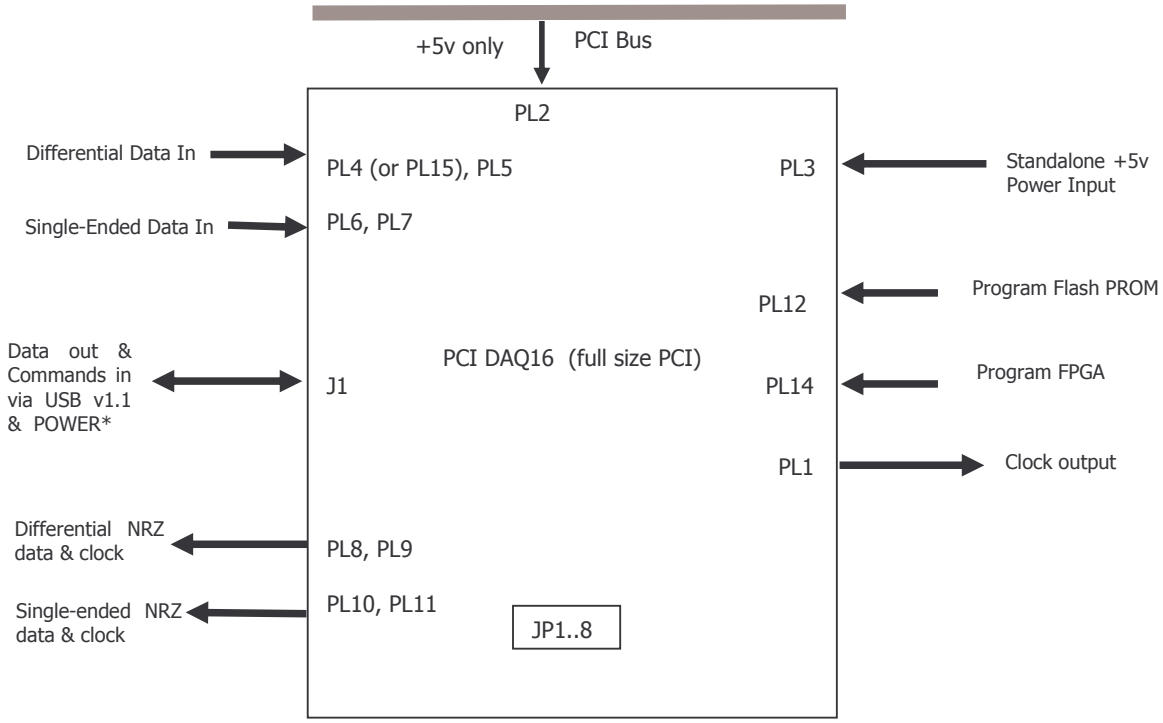


Figure 1: PCI DAQ16 Interfaces

* The USB interface may ONLY be used to POWER the DAQ if the output data and clock drivers are disabled and total current consumption of the DAQ is below 500mA.

2 Hardware Description

The PCI DAQ16 is a full height full length PCI board for use in a standard PC. The PCI interface is used only to provide the +5v power supply to the board. The board contains 3.3v and 2.5v voltage regulators to convert the input +5v supply. The DAQ also contains a 16Mbit FLASH PROM to configure the Altera field programmable gate arrays (FPGA), 1Mbytes of FIFO to buffer ~1.3s of sonobuoy data and a full-speed cypress USB v1.1 peripheral controller (EZ-USB-FX). All the required input signal conditioning and output buffers are also included. Buoy status LEDs are mounted on the edge of the DAQ to provide a visual indication of the buoy data status.

The PL4 and PL5 connectors are used for input of the 16 differential data and clock streams and PL6 and PL7 are used for the input of the single-ended (5v TTL) 16 data and clock signals. Differential (RS422 compatible) NRZ data and clock signals are available via PL8 and PL9 and the single-ended (5v TTL) NRZ data and clock signal can be output via connectors PL10 and PL11.

The FLASH PROM configures the FPGAs every time power is applied to the board. The DAQ can also be commanded to re-configure via a command message or by the user pressing the manual reset switch. The user may disable the flash PROM and configure the FPGAs directly using a download cable via PL14.

The user can control the operation and receive data from the DAQ in 2 groups of 8 channels. Windows 2000/XP USB driver SW is provided with sample code to enable ease of system integration.

The DAQ board may be mounted in a non-PC enclosure by fixing the DAQ board using the 5 mounting holes and using PL3 for +5v power input.

If the output signals are disabled, the DAQ can also be powered solely via the USB interface [NOTE: please see DAQ power requirements in section 3]

3 Power Requirements

The USB PCI DAQ16 board digital supply (+5v VDD) and digital ground (GND) are taken from the PCI connector. Power may also be supplied via PL3 or the USB interface (after setting jumper JP1).

The input current requirement is < 600mA from the +5V supply when the output drivers are disabled. The DAQ will consume more power if the outputs are enabled, the exact amount will depend upon the number and type of outputs used.

Voltage: +5v (PCI bus, USB bus or PL3)
Average current:: 450mA
Peak current: 600mA
Current : 2A (all outputs enabled)

4 Future Capability

The DAQ board uses large FPGAs to allow ease of upgrades and enhancements. The FPGA used have sufficient spare capacity to decode non-standard or experimental buoy frame types. Upgrades to the standard design can be easily implemented by downloading new FPGA configuration data into the Flash PROM (using an Altera download cable). The flash PROM can be re-programmed over 100,000 times. The SW in the EZ-USB-FX USB controller, which includes an 8051 micro-controller and 8 KB of on-chip RAM, is also downloaded when the user initializes the DAQ. This also allows ease of upgrade to the functionality of the DAQ.

5 Buoy Input and Output Signals

The DAQ board accepts differential data via PL4 (or PL15 if fitted) and PL5 and the single-ended data (+5v) via PL6 and PL7. USB command and header JP3 are used to control the input data path.

Differential (RS422) NRZ clock and data signals are output using PL8 and PL9. Single-ended (+5v) NRZ clock and data signals are available on PL10 and PL11. USB command and header JP4 controls the signals output.

Each 34-way IDC connector handles data for 8 channels and includes the clock and data signals for all 8 buoys.

5.1 Input Data

The input signal conditioning contains digital and RS422 receivers and will accept data from the following sources:

5.1.1 Data from "ARR-78" type radio receiver

Differential "TTL" data - clock signal not used.
High = +3.5±0.5v
Low = 0±0.5v
Impedance = 120Ω.

5.1.2 Data from 1" tape

Analogue 2V rms single ended (bipolar) – clock signal not used.
High = +2.8v
Low = -2.8v
Impedance = 50Ω.

5.1.3 Data from digital simulator

5v "TTL" data (with or without clock)
High = >+2.0v
Low = <+0.8v

5.1.4 Standard RS422 differential data

Differential signals with amplitude > 200mv

5.2 Output NRZ Clock and Data

The bit synchronized NRZ data and clock signals are output as standard +5v I/O (compatible with both +3.3v and +5.0v systems) with guaranteed V_{high} > 3.76v and V_{low} < 0.1v and/or as standard RS422 differential signals.

The effect of jumper JP3 on the data and clock phase relationship is shown in Figure 2.

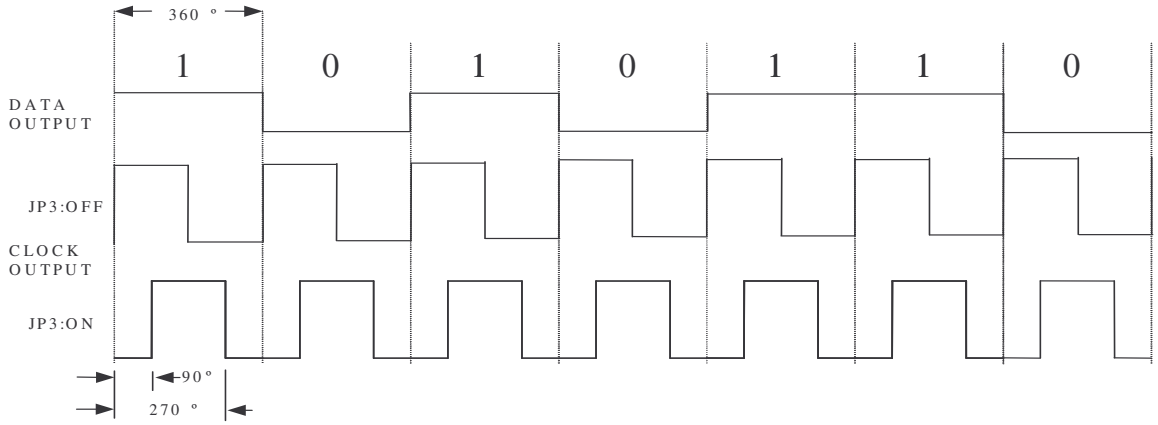


Figure 2: Output NRZ Data and Clock Signal Phase Relationship

5.3 Differential data input and output Connectors

All differential input and output signals are via male 34-pin IDC connectors (for use with 1.27mm [0.05"] ribbon cable) with pin-outs as follows:

Group 0 Input: PL4 (or PL15 if fitted)			
Group 0 Output: PL8			
Pin No	**Signal**	**Pin No**	**Signal**
1	GND	2	GND
3	Data 0 +	4	Data 0 -
5	Clock 0 +	6	Clock 0 -
7	Data 1 +	8	Data 1 -
9	Clock 1 +	10	Clock 1 -
11	Data 2 +	12	Data 2 -
13	Clock 2 +	14	Clock 2 -
15	Data 3 +	16	Data 3 -
17	Clock 3 +	18	Clock 3 -
19	Data 4 +	20	Data 4 -
21	Clock 4 +	22	Clock 4 -
23	Data 5 +	24	Data 5 -
25	Clock 5 +	26	Clock 5 -
27	Data 6 +	28	Data 6 -
29	Clock 6 +	30	Clock 6 -
31	Data 7 +	32	Data 7 -
33	Clock 7 +	34	Clock 7 -

Group 1 Input: PL5			
Group 1 Output: PL9			
Pin No	**Signal**	**Pin No**	**Signal**
1	GND	2	GND
3	Data 8 +	4	Data 8 -
5	Clock 8 +	6	Clock 8 -
7	Data 9 +	8	Data 9 -
9	Clock 9 +	10	Clock 9 -
11	Data 10 +	12	Data 10 -
13	Clock 10 +	14	Clock 10 -
15	Data 11 +	16	Data 11 -
17	Clock 11 +	18	Clock 11 -
19	Data 12 +	20	Data 12 -
21	Clock 12 +	22	Clock 12 -
23	Data 13 +	24	Data 13 -
25	Clock 13 +	26	Clock 13 -
27	Data 14 +	28	Data 14 -
29	Clock 14 +	30	Clock 14 -
31	Data 15 +	32	Data 15 -
33	Clock 15 +	34	Clock 15 -

Table 1: Differential Connectors Pin Details

5.4 Single-ended data input and output Connectors

All single-ended input and output signals are via male 34-pin IDC connectors (for use with 1.27mm ribbon cable) with pin-outs as follows:

Group 0 Input: PL6			
Group 0 Output: PL10			
Pin No	**Signal**	**Pin No**	**Signal**
1	GND	2	GND
3	Data 0 +	4	GND
5	Clock 0 +	6	GND
7	Data 1 +	8	GND
9	Clock 1 +	10	GND
11	Data 2 +	12	GND
13	Clock 2 +	14	GND
15	Data 3 +	16	GND
17	Clock 3 +	18	GND
19	Data 4 +	20	GND
21	Clock 4 +	22	GND
23	Data 5 +	24	GND
25	Clock 5 +	26	GND
27	Data 6 +	28	GND
29	Clock 6 +	30	GND
31	Data 7 +	32	GND
33	Clock 7 +	34	GND

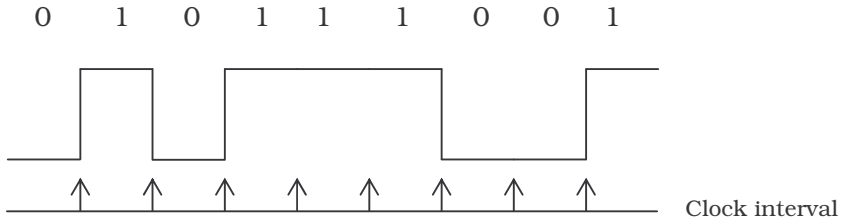
Group 1 Input: PL7			
Group 1 Output: PL11			
Pin No	**Signal**	**Pin No**	**Signal**
1	GND	2	GND
3	Data 8 +	4	GND
5	Clock 8 +	6	GND
7	Data 9 +	8	GND
9	Clock 9 +	10	GND
11	Data 10 +	12	GND
13	Clock 10 +	14	GND
15	Data 11 +	16	GND
17	Clock 11 +	18	GND
19	Data 12 +	20	GND
21	Clock 12 +	22	GND
23	Data 13 +	24	GND
25	Clock 13 +	26	GND
27	Data 14 +	28	GND
29	Clock 14 +	30	GND
31	Data 15 +	32	GND
33	Clock 15 +	34	GND

Table 2: Single-Ended Connector Pin Details

6 Input Data Encoding Schemes

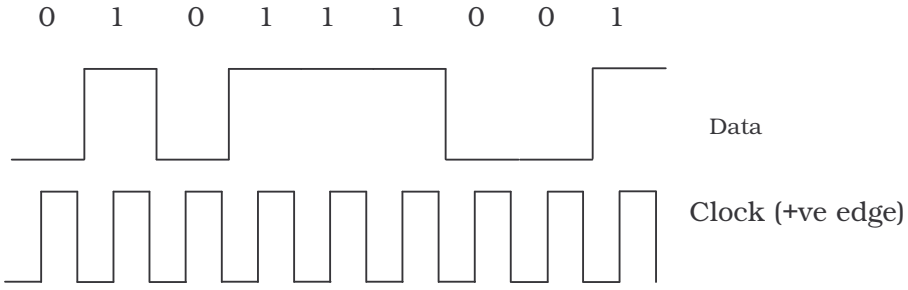
The following data encoding schemes are presently supported:

6.1 Non-return-zero (NRZ) – no clock



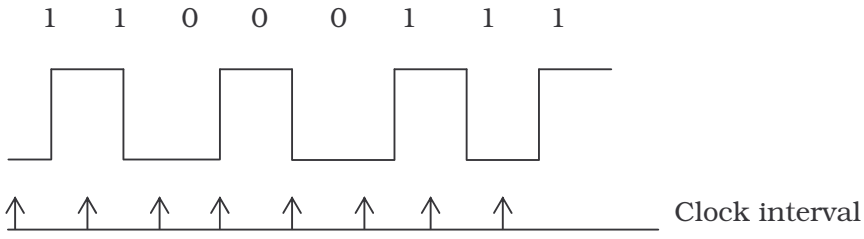
1 = high, 0 = low – transition only at the end of the clock interval

6.2 Non-return-zero (NRZ) – with clock



The clock detect edge can be selected as positive or negative.

6.3 Miller/DMM (delayed–modulation-mark) – no clock



1 = transition in middle of clock interval
0 = no transition at the end of the clock interval unless followed by a zero.

Others encoding schemes e.g. Bi-phase-L (Manchester) may be incorporated if required.

7 Jumper & Header Settings

7.1 DAQ Mode Selection

The jumpers JP1 to JP8 are used to set the mode of operation of the DAQ on power-up for both sets of 8 channels. Any set mode DAQ commands received via the USB interface take priority and the jumper settings will then be ignored and the mode specified in the USB command will be implemented.

The settings from JP1-8 will also be used after a STOP_ACQ command has been sent to the DAQ.

JP	Description	
	ON (down)	**OFF**
JP1	Use Clock Signal (only when data is NRZ)	Do NOT use Clock Signals
JP2	NRZ encoded input data	Miller/Bi-Φ-L encoded input data
JP3	Output - Advance NRZ output clock phase by 90 degrees♠	Output - Data edge on positive edge of clock
JP4	Serial test generator♦	Normal serial stream
JP5	Normal serial output	Faster serial output rate♥
JP6	When JP1 ON: Use positive clock edge	When JP1 ON: Use negative clock edge
JP7	*Buoy Specific*	*Buoy Specific*
JP8	*Buoy Specific*	*Buoy Specific*

Table 3: Jumper JP1-JP8 Settings

The user can control the mode of operation of each set of 8 channels independently.

Serial command formats are detailed in following sections.

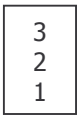
♠ JP3 must be ON to provide NRZ output data and clock phase comparable with "typical" radio receiver output signals.

♦ This is a test mode where the output is a counter – indicated by yellow LED ON – even when no signals present. The exact format of the test serial frame is buoy specific.

♥ This mode increases the expected buoy data rate to be that of the fastest buoy (within specification). The effect of this setting is that no data will be lost for even the fastest buoy but for buoys at the standard nominal rate, a ZERO frame will be inserted every N frames. NOTE: A zero frame will still contain the expected sync word but all other fields will be zero. A zero frame can be detected by checking the frame counter of the frame before and after and they should be consecutive numbers. Also there will only be 1 zero frame with frames before and after indicating good LOCK state.

7.2 Input Power Source Select

Header JP1 determines the source of the +5v power to the DAQ.



JP1

3-2: +5v power from the USB interface
2-1: +5v power from PCI interface [default]
Both open: +5v power via PL3

Caution: Extreme care must be taken to ensure that header JP1 is set up correctly otherwise the DAQ may be permanently damaged.

7.3 Input Signal Type Select

Header JP3 links 9-10 and 11-12 MUST be fitted.

The user can independently set the input data type for the lower [1-8] and upper [9-16] channels via USB command (see section **Error! Reference source not found.**). For example, channels 1-8 can be set for differential (RS422) input data and channels 9-16 can be set for single-ended (TTL) data.

NOTE: The user MUST only select either the differential or the single-ended signal types for each 8 channel group. Permanent damage may be caused if both types of inputs are selected for the same channel group.

INPUT SEL
JP3

2	4	6	8	10	12
1	3	5	7	9	11

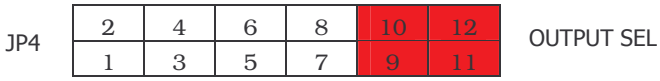
Header Pins	Description – Link fitted
1 – 2	Channels 1 – 8 differential : OPEN – enabled via USB command
3 – 4	Channels 9 – 16 differential: OPEN – enabled via USB command
5 – 6	Channels 1 – 8 TTL : OPEN – enabled via USB command
7 – 8	Channels 9 – 16 TTL : OPEN – enabled via USB command
9 – 10	Channels 1 – 8 : TTL Input direction IN* MUST BE SET
11 – 12	Channels 9 – 16 : TTL Input direction IN* MUST BE SET

** NOTE: These should ALWAYS be connected. The DAQ may be permanently damaged if these links are left open.*

7.4 Output Signal Type Select

Header JP4 links 9-10 and 11-12 MUST be fitted. If output signals are not required - do not enable either the single-ended of differential outputs.

The user can independently set the output data type for the lower [1-8] and upper [9-16] channels via USB command (see section **Error! Reference source not found.**). For example, channels 1-8 can be set for differential (RS422) output data and channels 9-16 can be set for single-ended (TTL) data.



Header Pins	Description – Link fitted
1 – 2	Channels 1 – 8 differential : OPEN – enabled via USB command
3 – 4	Channels 9 – 16 differential: OPEN – enabled via USB command
5 – 6	Channels 1 – 8 TTL : OPEN – enabled via USB command
7 – 8	Channels 9 – 16 TTL : OPEN – enabled via USB command
9 – 10	Channels 1 – 8 : TTL Output direction OUT* MUST BE SET
11 – 12	Channels 9 – 16 : TTL Output direction OUT* MUST BE SET

- *NOTE: These should ALWAYS be connected. The DAQ may be permanently damaged if these links are left open.*

7.5 FPGA Program Select

Header JP7 controls whether the Altera FPGAs are programmed in parallel (both FPGA loaded with same image) or serial (each group of 8 channels may be configured to handle data from different buoys). The 16Mbit FLASH PROM has sufficient capacity to hold images for 4 FPGAs. If the FPGAs are programmed serially (default) then only 2 independent DAQ configurations are possible. If the FPGAs can be programmed in parallel (both groups are programmed with the same image) then 4 independent DAQ configurations can be stored on the FLASH PROM.

1-2: Program FPGAs in parallel
2-3: Program FPGA1 and then FPGA2 – serial [default]
Both open: Invalid option

7.6 Program FPGAs from FLASH PROM Select

All links on header JP5 must be connected to use the on-board Flash PROM to configure the FPGAs.

JP5

	Description	
Header Pins	**Configure FPGAs using FLASH PROM**	**Configure FPGAs using download cable**
1 – 2	SET	OPEN
3 – 4	SET	OPEN
5 – 6	**THIS LINK MUST BE CONNECTED IN BOTH MODES**	
7 – 8	SET	OPEN
9 - 10	SET	OPEN

7.7 Reset Switch

The DAQ indicates successfully power up and programming of the FPGAs by a yellow flashing LED for each group. If the DAQ fails to power up, a reset switch (located next to PL15) may be used to force a hardware reset of both the EZ-USB-FX USB controller and the FPGAs on the DAQ. When the switch is released, the FPGA will then reload configuration data from the PROM and the PC host must re-initialize the USB driver – this will normally require the USB cable to the DAQ to be un-plugged and re-inserted.

8 USB Interface

The DAQ board has a full-speed (12MHz) USB v1.1 interface and to guarantee error-free and continuous data transfer from the DAQ, there MUST not be any other USB device in the USB chain on the same USB hub. The DAQ also contains 1Mbytes of FIFO storage to buffer the data from each group of 8 channels and pass onto the PC host when requested. The data is transferred when the PC issues USB BULK-IN data requests.

8.1 USB Data Format

This section is included only for information. The user is not required to be familiar with this format information and the supplied PCI-DAQ16 Application programming Interface (API) allows the user to fully configure the DAQ and access to all buoy data.

The data from each group of 8 channels is multiplexed into a single data stream before being transferred to the PC. The PC host SW requests data from one or both groups, as required.

8.1.1 Multiplexed data stream

The 32 bit buoy data (per group of 8 channels) is multiplexed into a single stream as follows:

Address (hex)	0 1 2 3	4 5 6 7	8 9 A B	C D E F
0000-F	Channel 0 word 0	Channel 1 word 0	Channel 2 word 0	Channel 3 word 0
0010-F	Channel 4 word 0	Channel 5 word 0	Channel 6 word 0	Channel 7 word 0
0020-F	Channel 0 word 1	Channel 1 word 1	Channel 2 word 1	Channel 3 word 1
0030-F	Channel 4 word 1	Channel 5 word 1	Channel 6 word 1	Channel 7 word 1
0040-F	Channel 0 word 2	Channel 1 word 2	Channel 2 word 2	Channel 3 word 2
0050-F	Channel 4 word 2	Channel 5 word 2	Channel 6 word 2	Channel 7 word 2
0060-F	.....	....	.....	....

Table 4: Multiplexed Data Stream

Each channel word is 4 bytes long defined as follows [little endian]:

32 bit word			
MSB BIT[31:24]	BIT[23:16]	BIT [15:08]	BIT [07:00] LSB
BYTE 03	BYTE 02	BYTE 01	BYTE 00

Table 5: 32 bit word format

8.1.2 Serial frame word format

The DAQ output serial frame format is buoy specific and is detailed in the relevant buoy specific document.

9 Output Clock Signals

A 16-way 0.1" standard IDC connector for use with 0.05" pitch ribbon cable is used to output the CLK signals as well as to input user specific signals. All input and output signals are TTL buffered. The connector pin-outs are detailed below:

Pin No	Signal	Pin No	Signal
1	*+5V output*	2	GND
3	Output CLK FPGA2	4	Output CLK FPGA1
5	*SP3_OUT*	6	*SP2_OUT*
7	GND	8	GND
9	*SP1_IN*	*10*	*SP0_IN*
11	*SP3_IN*	*12*	*SP2_IN*
13	*RxD input*	*14*	*TxD output*
15	*+3.3v output*	16	GND

Table 6: Test Connector Details (PL1)

Signals in italics are used for test purposes but may be used to provide extra user functionality if required.

10 Environmental

The standard PCI-DAQ16 card has been manufactured using commercial temperature (0 to 70˚C) grade components for use in standard PC environments.

For use in more harsh environments, the PCI-DAQ16 can be manufactured using industrial temperature grade components – details are available on request.

The use of surface mount components results in a higher reliability and low failures due to mechanical shock.

10.1 Mechanical

The DAQ16 card is a full length full height standard PCI card (312 x 107mm) and occupies a single slot in a standard PC.

The DAQ16 board may also be integrated into a non-standard non-PC enclosure by using the 5 fixing holes.

10.2 Temperature

Operating Temperature: 0° to 60º C

Storage Temperature: -40° to 70° C

Humidity: 0 - 90% con-condensing

11 Status Indicators

The status of the DAQ board and data being processed is displayed using a row of LEDs mounted on side 2 of the board.

The following status information is displayed:

LED	COLOUR	STATUS	DESCRIPTION
DL1	RED	OFF	Buoys 1 – 8 FIFO Not FULL – data valid
		FLASHING	Buoys 1 – 8 FIFO FULL – data being discarded
DL2	RED	OFF	Good data Streams from buoys 1 to 8
		ON	Status error – buoy specific
DL3 – DL10	GREEN	OFF	Invalid Buoy n Signal
		ON	FRAME SYNC on Buoy n – valid signal
		FLASHING	Data stream with errors
DL11	YELLOW	OFF	Buoys 1 – 8 FPGA Not Configured
		ON♦	Buoys 1 – 8 FPGA configured – valid data on a channel
		FLASHING ~1Hz	Buoys 1 – 8 FPGA configured – but no FRAME SYNC on any buoy channel 1 to 8
DL12	RED	OFF	Buoys 9 – 16 FIFO Not FULL – data valid
		FLASHING	Buoys 9 – 16 FIFO FULL – data being discarded
DL13	RED	OFF	Good data Streams from buoys 9 to 16
		ON	Status error – buoy specific
DL14 – DL21	GREEN	OFF	Invalid Buoy Signal on channel n
		ON	FRAME SYNC on Buoy n – valid signal
		FLASHING	Data stream with errors
DL22	YELLOW	OFF	Buoys 9 – 16 FPGA Not Configured
		ON♦	Buoys 9 – 16 FPGA configured – valid data on a channel
		FLASHING ~1Hz	Buoys 9 – 16 FPGA configured – but no FRAME SYNC on any buoy channel 9 to 16
DL23	GREEN	OFF	No HW USB connection
		ON	USB HW connection established

Table 7: USB PCI DAQ status LEDs

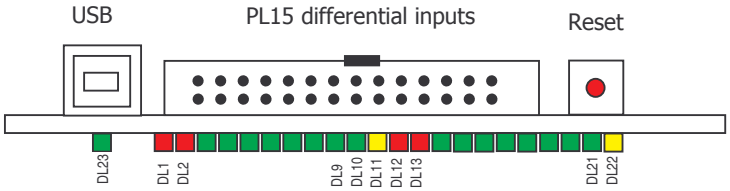


Figure 3: View of IDC and USB Connectors and status LEDs

♦ Also signifies SERIAL TEST mode

12 Hardware Installation

CAUTION: *The DAQ contains Electro-static discharge (ESD) sensitive devices. All standard ESD handling precautions must be taken during installation/removal of the board, taking proper precautions to ground yourself and the work area before removing the board from its anti-static bag. Failure to follow proper handling procedures could result in permanent damage.*

This section details all the headers that must be set up before power is applied to the DAQ. It is strongly recommended that the user read this section fully before working with the DAQ.

- The following links MUST be connected at ALL times:

  JP3: 9-10 & 11-12 - Ensures no conflict of input source signals

  JP4: 9-10 & 11-12 - Ensures no conflict of output source signals

  JP5: 5-6 - Ensures route of nCONFIG signals for FPGAs

  These links are normally coloured [RED or BLUE] for ease of recognition and clarity.

- Select the DAQ power source – JP1 – detailed in section 7.2.
- Set the FPGA configuration mode – JP7 – detailed in section 7.5.
- Select the power-up DAQ mode using the jumper setting – S1 – detailed in section 7.1. NOTE: These settings will be ignored once the DAQ mode command has been sent via the USB.
- Select input signal type via USB command – JP3 – all open (except 9-10 & 11-12).
- Select output signal type via USB command – JP4 – all open (except 9-10 & 11-12).
- Power down the PC.
- Fit the DAQ into a spare PCI slot inside the PC – following all standard ESD precautions.
- Power up the PC. If the DAQ has been set to configure the FPGAS using the on-board FLASH PROM then the two yellow LEDs should start to flash indicating correct FPGA configuration and power-up self test.
- Connect the USB cable between the PC and the DAQ. The PC should signal the presence of the DAQ as a “Devana Systems PCI DAQ16 USB Driver” – under the USB menu of the Device Manager in System properties [Windows 2000/XP].
- The DAQ HW is now ready.